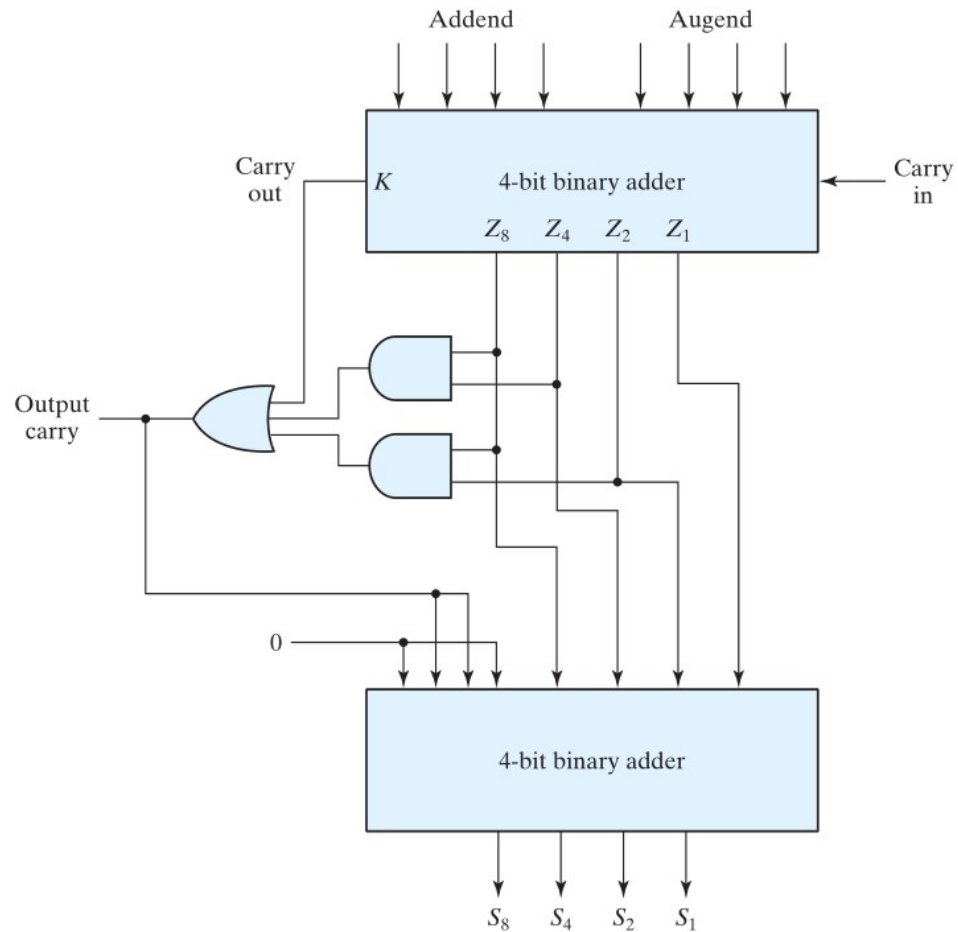


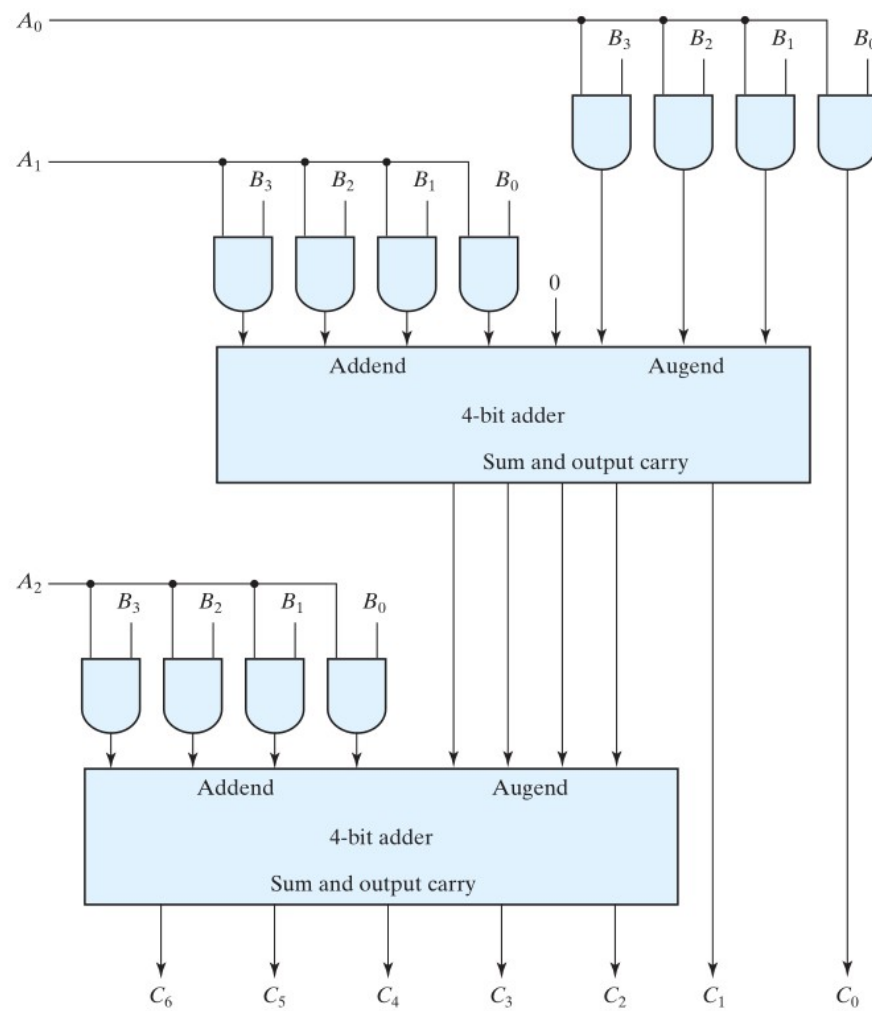
- 4.18** Design a combinational circuit that generates the 9's complement of a
- (a) \* BCD digit. (HDL—see Problem 4.54(a).)
  - (b) Gray-code digit. (HDL—see Problem 4.54(b).)

**4.19** Construct a BCD adder-subtractor circuit. Use the BCD adder of Fig. 4.14 and the 9's complementer of problem 4.18. Use block diagrams for the components. (HDL—see Problem 4.55.)



**FIGURE 4.14**  
Block diagram of a BCD adder

- 4.20** For a binary multiplier that multiplies two unsigned four-bit numbers,  
(a) Using AND gates and binary adders (see Fig. 4.16), design the circuit.



**FIGURE 4.16**  
Four-bit by three-bit binary multiplier

- 4.21** Design a combinational circuit that compares two 4-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.

**4.22\*** Design an excess-3-to-binary decoder using the unused combinations of the code as don't-care conditions. (HDL—see Problem 4.42.)

- 4.25** Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4-line decoder. Use block diagrams for the components. (HDL—see Problem 4.63.)

**4.28** Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions:

(a)  $F_1 = x'yz' + xz$

$$F_2 = xy'z' + x'y$$

$$F_3 = x'y'z' + xy$$

(b)  $F_1 = (y' + x)z$

$$F_2 = y'z' + x'y + yz'$$

$$F_3 = (x + y)z$$

- 4.29\*** Design a four-input priority encoder with inputs as in Table 4.8, but with input  $D_0$  having the highest priority and input  $D_3$  the lowest priority.

**Table 4.8**  
*Truth Table of a Priority Encoder*

Inputs				Outputs		
$D_0$	$D_1$	$D_2$	$D_3$	$x$	$y$	$V$
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1



- 4.31** Construct a  $16 \times 1$  multiplexer with two  $8 \times 1$  and one  $2 \times 1$  multiplexers. Use block diagrams. (HDL—see Problem 4.67.)

**4.32** Implement the following Boolean function with a multiplexer (HDL—see Problem 4.46):

(a)  $F(A, B, C, D) = \Sigma(0, 2, 5, 8, 10, 14)$

(b)  $F(A, B, C, D) = \Pi(2, 6, 11)$

**4.34** An  $8 \times 1$  multiplexer has inputs  $A$ ,  $B$ , and  $C$  connected to the selection inputs  $S_2$ ,  $S_1$ , and  $S_0$ , respectively. The data inputs  $I_0$  through  $I_7$  are as follows:

(a)\*  $I_1 = I_2 = I_7 = 0$ ;  $I_3 = I_5 = 1$ ;  $I_0 = I_4 = D$ ; and  $I_6 = D'$ .

(b)  $I_1 = I_2 = 0$ ;  $I_3 = I_7 = 1$ ;  $I_4 = I_5 = D$ ; and  $I_0 = I_6 = D'$ .

**4.35** Implement the following Boolean function with a  $4 \times 1$  multiplexer and external gates.

(a)\*  $F_1(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$

(b)  $F_2(A, B, C, D) = \Sigma(1, 2, 5, 7, 8, 10, 11, 13, 15)$

Connect inputs  $A$  and  $B$  to the selection lines. The input requirements for the four data lines will be a function of variables  $C$  and  $D$ . These values are obtained by expressing  $F$  as a function of  $C$  and  $D$  for each of the four cases when  $AB = 00, 01, 10$ , and  $11$ . These functions may have to be implemented with external gates. (HDL—see Problem 4.47.)