

- 6.2** Include a synchronous clear input to the register of Fig. 6.2. The modified register will have a parallel load capability and a synchronous clear capability. The register is cleared synchronously when the clock goes through a positive transition and the clear input is equal to 1. (HDL—see Problem 6.35(a), (b).)

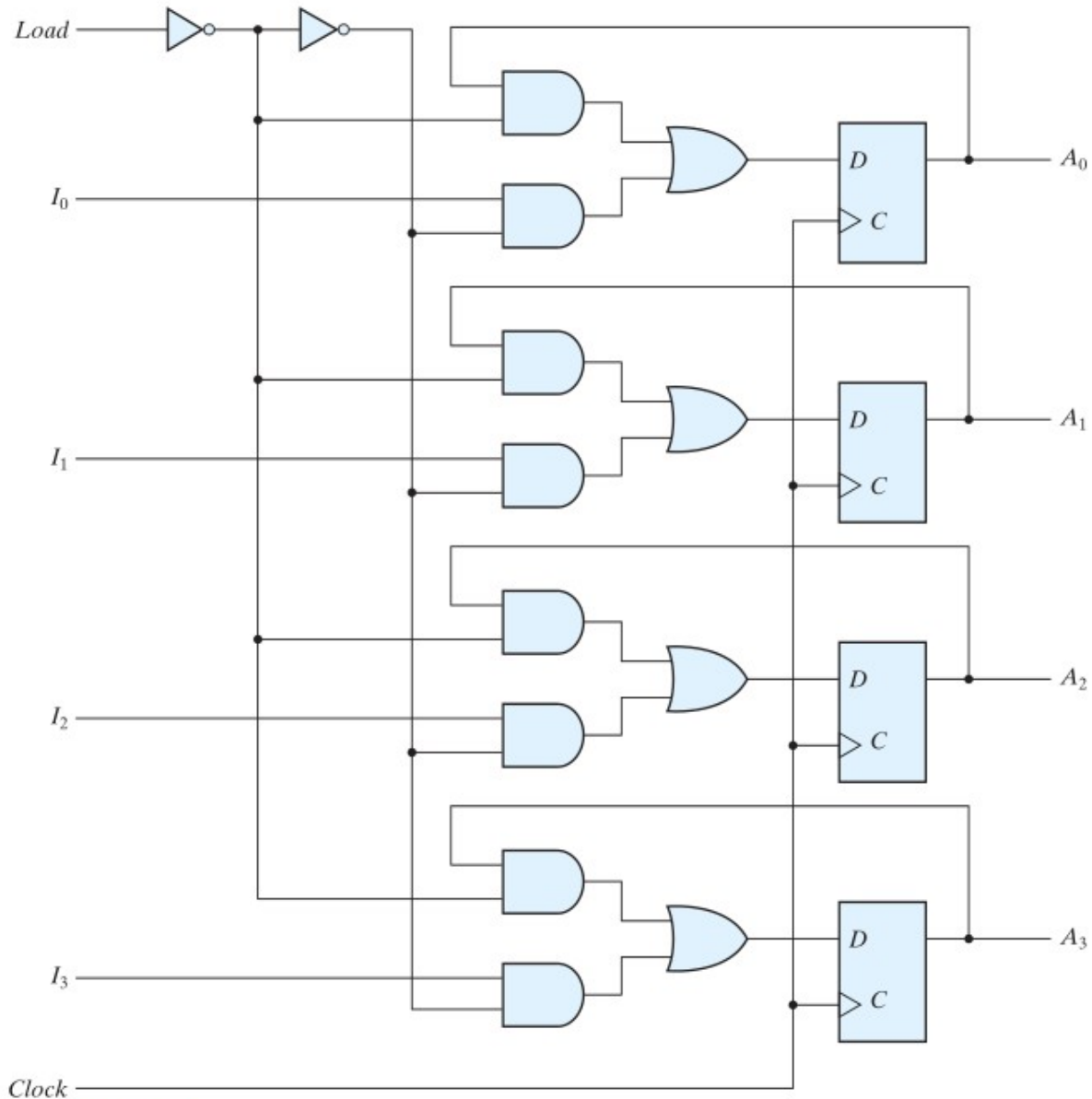
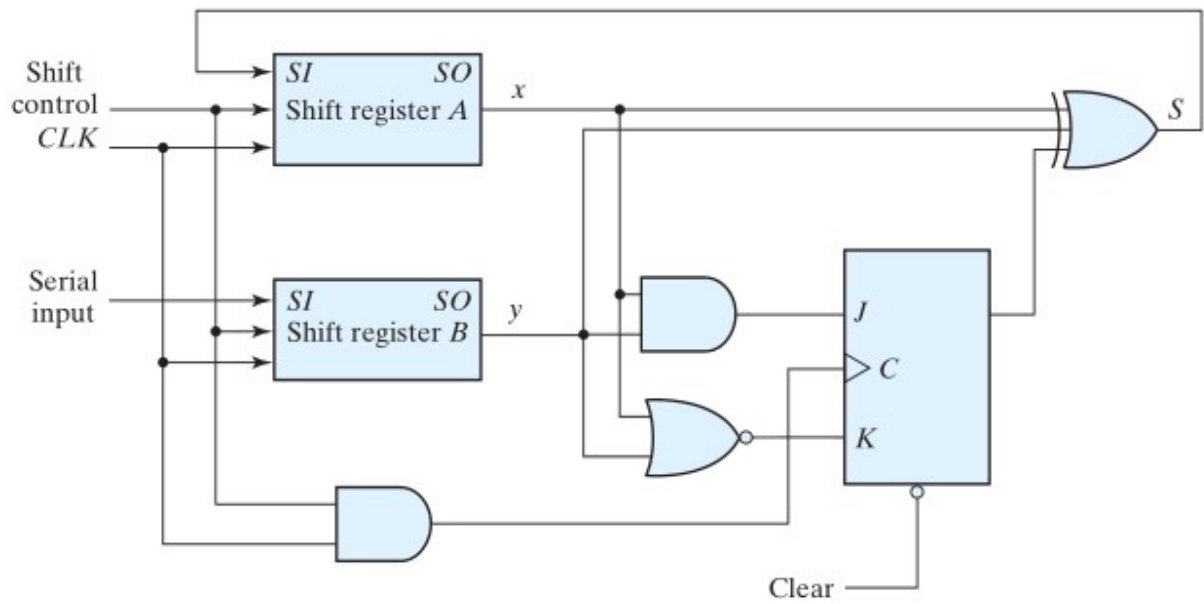


FIGURE 6.2
Four-bit register with parallel load

- 6.4*** The contents of a four-bit register is initially 0110. The register is shifted six times to the right with the serial input being 1011100. What is the content of the register after each shift?

- 6.8*** The serial adder of Fig. 6.6 uses two four-bit registers. Register *A* holds the binary number 0101 and register *B* holds 0111. The carry flip-flop is initially reset to 0. List the binary values in register *A* and the carry flip-flop after each shift. (HDL—see Problem 6.54).



- 6.9** Two ways for implementing a serial adder ($A + B$) is shown in Section 6.2. It is necessary to modify the circuits to convert them to serial subtractors ($A - B$).
- (a) Using the circuit of Fig. 6.5, show the changes needed to perform $A + 2$'s complement of B . (HDL—see Problem 6.35(h).)
 - (b) *Using the circuit of Fig. 6.6, show the changes needed by modifying Table 6.2 from an adder to a subtractor circuit. (See Problem 4.12). (HDL—see Problem 6.35(i).)

- 6.6** Design a four-bit shift register with parallel load using D flip-flops. There are two control inputs: *shift* and *load*. When *shift* = 1, the content of the register is shifted by one position. New data are transferred into the register when *load* = 1 and *shift* = 0. If both control inputs are equal to 0, the content of the register does not change. (HDL—see Problem 6.35(c), (d).)

- 6.7** Draw the logic diagram of a four-bit register with four D flip-flops and four 4×1 multiplexers with mode selection inputs s_1 and s_0 . The register operates according to the following function table. (HDL—see Problem 6.35(e), (f).)

s_1	s_0	Register Operation
0	0	No change
1	0	Complement the four outputs
0	1	Clear register to 0 (synchronous with the clock)
1	1	Load parallel data

- 6.11** A binary ripple counter uses flip-flops that trigger on the positive-edge of the clock. What will be the count if
- (a) the normal outputs of the flip-flops are connected to the clock and
 - (b) the complement outputs of the flip-flops are connected to the clock?

- 6.12** Draw the logic diagram of a four-bit binary ripple countdown counter using
- (a) flip-flops that trigger on the positive-edge of the clock and
 - (b) flip-flops that trigger on the negative-edge of the clock.

- 6.13** Show that a BCD ripple counter can be constructed using a four-bit binary ripple counter with asynchronous clear and a NAND gate that detects the occurrence of count 1010. (HDL—see Problem 6.35(k).)

6.17* Design a four-bit binary synchronous counter with D flip-flops.

6.22 For the circuit of Fig. 6.14, give three alternatives for a mod-10 counter (i.e., the count evolves through a sequence of 12 distinct states).

- Using an AND gate and the load input.
- Using the output carry.
- Using a NAND gate and the asynchronous clear input.

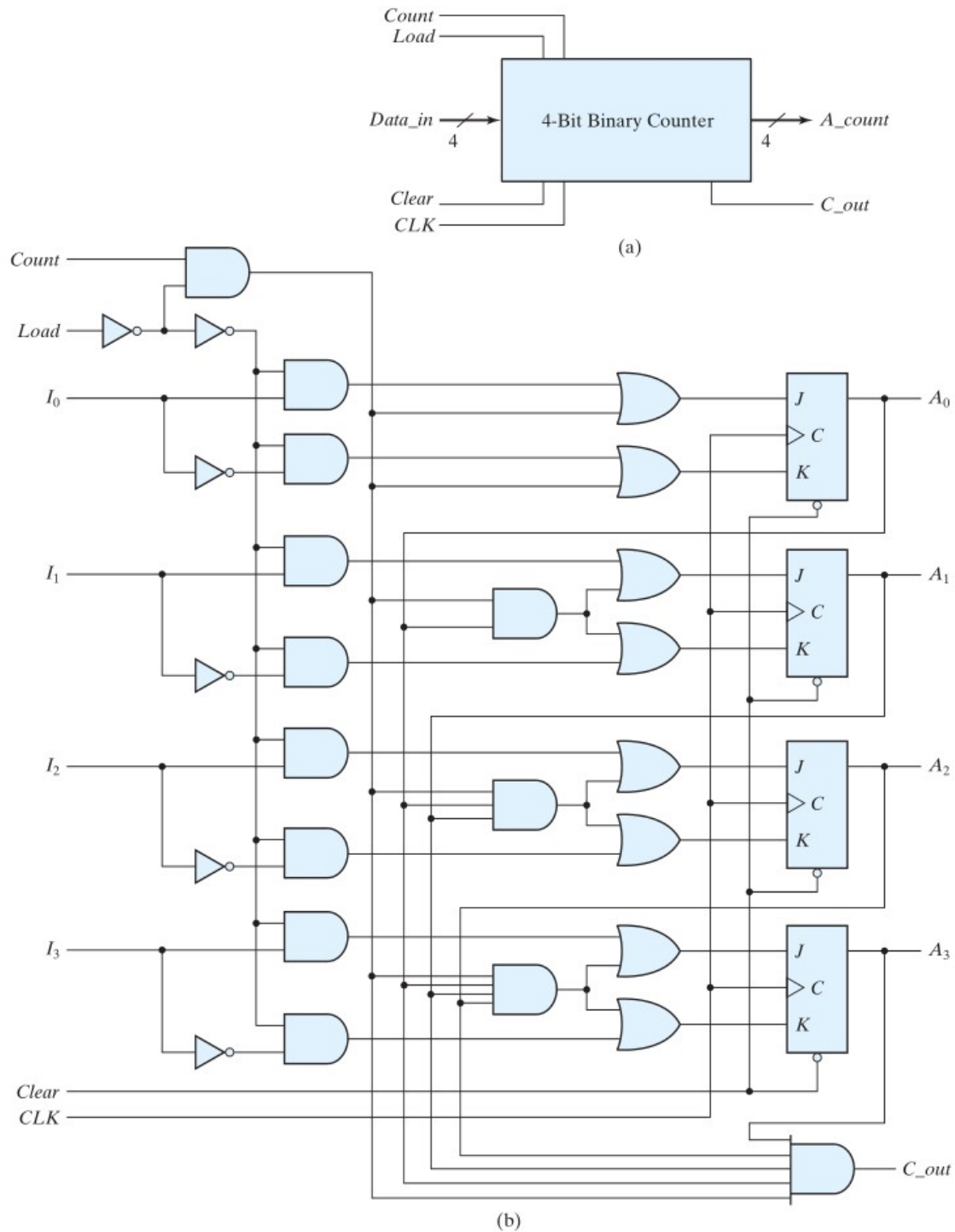


FIGURE 6.14

6.27 Using JK flip-flops,

- (a) Design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6.
(HDL—see Problem 6.50(a), 6.51.).
- (b) Draw the logic diagram of the counter.

6.28 Using *D* flip-flops,

- (a) *Design a counter with the following repeated binary sequence: 0, 1, 2, 4, 6. (HDL—see Problem 6.50(b).)
- (b) Draw the logic diagram of the counter.
- (c) Design a counter with the following repeated binary sequence: 0, 2, 4, 6, 8.
- (d) Draw the logic diagram of the counter.

